**ELEC 204 Digital Design Preliminary Lab Report**

Preliminary Lab 1

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Date: (10/10/2019)

\*Please delete the highlighted lines and write your own parts for the report.

\*\*Reminder: Your lab grade is a weighted average of your performance before, during and after the lab: **Total lab grade = Preliminary work\* (20%) + Lab interview and demo\* (40%) + Lab report (20%)**

**\*\*\*Please make sure the preliminary report does not exceed 2 A4 pages.**

For the preliminary work, please provide here:

**QUESTION 4.1**

***K-MAP for AG***

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| B0 B1 B2/A0 A1 A2 | 000 | 001 | 011 | 010 | 100 | 101 | 111 | 110 |
| 000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 001 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 011 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| 010 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 100 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 101 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| 111 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 110 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |

*Prime implicants are shown above as much as Microsoft Word allows. At the end, expression for AG becomes:*

***(A0)(B0’) + (A1)(B0’)(B1’) + (A0)(A1)(B1’) + (A2)(B0’)(B1’)(B2’) + (A1)(A2)(B0’)(B2’) + (A0)(A2)(B1’)(B2’) + (A0)(A1)(A2)(B2’)***

*When we simplify this by using XNOR gates and common literals, expression becomes:*

*A2(B2’) + (A2⊕B2)’[A1B1’ + (A1⊕B1)’(A0B0’)]*

***K-MAP FOR BG***

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| B0 B1 B2/A0 A1 A2 | 000 | 001 | 011 | 010 | 100 | 101 | 111 | 110 |
| 000 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 001 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 011 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 010 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| 100 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 101 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 111 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 110 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

*When we look at the values, we can see that every value is the symmetry of the corresponding value in the previous k-map. By grouping prime implicants similarly, the expression for BG becomes:*

***(A1’)(B1) + (A2’)(B1)(B2) + (A1’)(A2’)(B2) + (A2’)(B1)(B2)(B2) + (A2’)(A2’)(B1)(B2) + (A1’)(A2’)(B2)(B2) + (A1’)(A2’)(A2’)(B2)***

*When we simplify this by using XNOR gates and common literals, expression becomes:*

*B2A2’ + (A2⊕B2)’[A1’B1+(A1⊕B1)’(B0A0’)]*

***K-MAP for EQ***

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| B0 B1 B2/A0 A1 A2 | 000 | 001 | 011 | 010 | 100 | 101 | 111 | 110 |
| 000 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 001 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 011 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 010 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 100 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 101 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 111 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 110 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

*For this k-map, we have to express every minterm by itself, therefore the simplest expression is rather complex.*

However, we can represent EQ as:

***EQ = (AG OR BG)’***

*Or we can think of this as comparing bit by bit and looking if all bits are equal:*

*(A1 ⊕ B1)’ (A2 ⊕ B2)’ (A2 ⊕ B2)'*

QUESTION 4.2

**LOGIC CIRCUIT EQ**

A1

B1

A2

B2

A0

B0

LOGIC CIRCUIT AG

A0

B0’

A1

B1

A1

B1’

B2

A2

A2

B2’

Logic Circuit BG

A0’

B0

A1

B1

A1’

B1

B2

A2

A2’

B2

AND OR

XNOR

**ELEC 204 Digital Design Lab Report**

Lab XX

Name: Student Name

Date: date of submission on blackboard (MM/DD/YYYY)

\*Please delete the highlighted lines and write your own parts for the report.

\*\*Reminder: Your lab grade is a weighted average of your performance before, during and after the lab: **Total lab grade = Preliminary work\* (20%) + Lab interview and demo\* (40%) + Lab report (20%)**

**\*\*\*Please make sure the lab report does not exceed 4 A4 pages.**

\*\*\*\*Please make sure you indicate the name of your lab collaborator (if there is any) who you worked together to solve the lab questions. Do not change your lab collaborator throughout the semester.

1. **Introduction and objectives**

Explain the objectives of the lab (refer to the lab instruction sheet),

Explain what your code has to do and describe how you did it.

1. **Methods**

Explain the inputs (how many bits, names of the inputs),

Explain the outputs (how many bits, names of the outputs),

Explain what the VHDL code must do

Explain how your code works

Provide the truth table

1. **Problems encountered, errors and warnings resolved**

Explain what problems you encountered while writing your code.

Explain what synthesis errors and warnings you observed.

Explain what problems you had to solve (or could not) on your board even if your code could be synthesized successfully.

1. **Conclusion**

Provide a 1 paragraph summary of the lab and explain what you learned from this lab.

References

1. Please cite any resource (web site, book, youtube video) you used for this lab.

**Appendix 1. Lab source code**

**Appendix 2. RTL schematics**

**Appendix 2. FPGA Board photos showing working code**

**Appendix 4. Screenshots from Xilinx for the errors and other board issues**